In the Specification

At page 1, lines 8 – 10, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

This application claims the benefit of U.S. Provisional Application Serial No. 60/102,865, filed on October 2, 1998 ~~(STFD.005P1)~~, and entitled "Noise-Reducing Arrangement And Method For Signal Processing."

At page 11, lines 21 – 23 and page 12, lines 1 - 13, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

In applications where the incoming or outgoing data does not need to be processing data on a full-time basis, certain example implementations of the present invention permit can be particularly advantageous. Consider, for example, reading data from a disc drive, or writing data to a disc drive. In the reading application, the analog circuitry can be used to read and store into a large memory portions of disc drive data while the high-speed digital circuitry is on for only those small periods of time necessary to extract and process the stored data for later use. As the large memory begins to fill, the reading cycle from the disc drive is paused while the high-speed digital circuitry extracts and processes the stored data. Alternatively, as the large memory begins to fill, the location on the disc drive for data already read into the memory is recorded for subsequent reading by the analog circuitry so as to permit access and extraction of the data in memory by the high-speed digital circuitry. This is one ~~of~~of a number of example data-transfer applications, where the proportions of on and off time for the analog and digital circuitry are not critical and the application can permit variances of the digital circuitry being on or off for more than fifty percent of the time with the analog circuitry being off or on for the remaining time.

At page 13, lines 17 – 23 and page 14 lines 1 - 7, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

In large mixed-signal systems, significant digital switching noise couples to the substrate, seriously affecting sensitive analog circuits. This can result in self-jamming of the GPS receiver. Partitioning the analog acquisition and digital processing into separate blocks of time eliminates the effects of the digital noise. According to a specific implementation of the present invention, a memory circuit is used to store acquired data that is to be processed when the digital section is subsequently re-enabled (or reactivated). The memory, which can be a digital circuit or an analog circuit, is designed to generate as little substrate noise as possible, minimizing the interference to the analog front end. For instance, one memory implementation uses a large block of small-scaled memory cells that do not require a noisy refresh circuit. Another more specific implementation of such a memory cell block is described and illustrated in connection with U.S. Patent Application No. 09/092,449, filed June 5, 1998 ~~(STFD.03PA)~~, now U.S. Patent No. 6,229,161 and entitled "Semiconductor Current-Switching Device Having Operations Enhancer and Method Therefor," incorporated herein by reference in its entirety.